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Gate-Controlled Spin-Orbit Interaction in InAs High-Electron Mobility Transistor Layers Epitaxially Transferred onto Si Substrates

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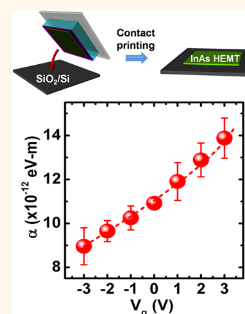
ABSTRACT We demonstrate gate-controlled spin-orbit interaction (SOI) in InAs high-electron mobility transistor (HEMT) structures transferred epitaxially onto Si substrates. Successful epitaxial transfer of the multilayered structure after separation from an original substrate ensures that the InAs HEMT maintains a robust bonding interface and crystalline quality with a high electron mobility of 46200 $cm^2/(V\ s)$ at 77 K. Furthermore, Shubnikov-de Haas (SdH) oscillation analysis reveals that a Rashba SOI parameter (α) can be manipulated using a gate electric field for the purpose of spin field-effect transistor operation. An important finding is that the α value increases by about 30% in the InAs HEMT structure that has been transferred when compared to the as-grown structure. First-principles calculations indicate that the main causes of the large improvement in α are the bonding of the InAs HEMT active layers to a SiO_2 insulating layer with a large band gap and the strain relaxation of the InAs channel layer during epitaxial transfer. The experimental results presented in this study offer a technological platform for the integration of III–V heterostructures onto Si substrates, permitting the spintronic devices to merge with standard Si circuitry and technology.



KEYWORDS: spin field-effect transistor · epitaxial transfer · spin-orbit interaction · high-electron mobility transistor · selective wet-etching

Spintronics utilizes the spin degree of freedom of electrons as well as charge and finds a wide range of applications from logic to storage devices.[1] The Rashba spin-orbit interaction (SOI) is particularly important in spintronic devices, such as the spin field-effect transistor (spin-FET).[2,3] Recently, III–V compound semiconductors (CSs), such as InGaAs, InAs, and InSb, with a significantly larger *g*-factor, high electron mobility, and strong SOI, have attracted much attention as channel materials in spin-FETs.[3–5] One of the challenges in the development of spin-FETs is the heterogeneous integration of devices onto Si substrates, allowing III–V CS spintronics to be incorporated into existing Si semiconductor technology. For the similar purpose, technologies have been developed for the growth of magnetic tunnel junctions (MTJs) on Si substrates. Furthermore, the MTJ-based memory could then be integrated with Si complementary metal-oxide-semiconductor (CMOS) logic circuit in order to realize future universal large-scale integration (LSI) circuits.[6,7]

The heterogeneous integration of III–V CSs onto different substrates, including Si, glass, and flexible polymer substrates, has given rise to various potential applications that are not possible using conventional devices built on III–V CS substrates.[8–16] Due to the excellent electron mobility, a light electron effective mass, and efficient light emission/detection,[15–18] the III–V CS has been used widely in metal-oxide-semiconductor field-effect transistors (MOSFETs), light-emitting diodes (LEDs), and solar cells on heterogeneous substrates.[19–25] To date, there have been numerous attempts to integrate III–V CSs onto Si substrates. Direct growth of epitaxial III–V CSs on Si *via*

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strain-engineered growth techniques has been pursued for over three decades for use in large-area electronics.[19,26] However, the relatively thick buffer layer and the interfacial defects resulting from the large lattice mismatch between III−V CSs and Si are considered as an inevitable obstacle. In apparent contrast, the selective etching of a sacrificial layer followed by the transfer of epitaxially grown III−V CS layers provides an alternative strategy that is free from the issues related to the lattice mismatch, thereby allowing integration of III−V CSs onto arbitrary host substrates including a Si substrate.[27,28] Although epitaxial transfer technology has been successfully applied for single layers of III−V CSs, multilayer transfer remains a great challenge due to the low selective etching capability for multiple material compositions in III−V CS heterostructures. The successful transfer of III−V heterostructures onto Si substrates may potentially lead to groundbreaking III−V CS devices such as high-electron mobility transistors (HEMTs) and spin-FETs integrated onto Si substrates.

In this study, we report the promising integration of InAs HEMT structures onto a Si substrate by using an epitaxial transfer technique and demonstrate gate-controlled SOI for potential spin-FET applications. In the epitaxial transfer technique, the pseudomorphic InAs HEMT structures grown on InP substrates are transferred onto Si substrates by employing a contact printing method after selective wet-etching of an InP substrate and buffer layers without destroying the active InAs HEMT structures. Furthermore, we found stronger gate electric field (V_g) dependence of the Rashba SOI in the transferred InAs HEMT structure. This is an essential factor in the realization of the spin-FET and demonstrates the potential feasibility of epitaxial transfer techniques to integrate III−V CS spintronic devices onto Si substrates.

RESULTS AND DISCUSSION

Figure 1a shows a schematic of the procedures used for the epitaxial transfer of a pseudomorphic InAs HEMT structure from an InP substrate onto a Si substrate. The InAs HEMT structures used in this study were epitaxially grown on InP (001) substrates using a solid-source molecular beam epitaxy (MBE) system. A schematic of the as-grown InAs HEMT structure is depicted in Figure 1b and it was integrated onto a Si substrate using the epitaxial transfer technique. The epitaxial transfer method consists of the selective wet-etching of an InP substrate and a buffer layer to separate the InAs HEMT active layers and the controlled transfer of the active layers onto a SiO_2/Si substrate by using a contact printing process.[10,27] One of the critical requirements during the selective wet-etching process is the protection of $In_{0.52}Al_{0.48}As$ layers included in the InAs HEMT active layers, except the 300 nm thick $In_{0.52}Al_{0.48}As$ buffer layer, because they can easily be etched in a hydrochloric acid (HCl)-based wet-etching solution. Therefore, we employed a poly(methyl methacrylate) (PMMA) coating layer on top of an elastomeric poly(dimethylsiloxane) (PDMS) stamp for the partial embedment of the InAs HEMT active layers (Figure S1, Supporting Information). In this process, a PMMA solution was spin-coated on the PDMS stamp, the as-grown InAs HEMT structure was gently pressed into the PMMA film, and the InP substrate and $In_{0.52}Al_{0.48}As$ buffer layer were selectively etched in HCl solution. Here, the elastomeric PDMS stamp provides conformal contacts between the HEMT layer and Si substrates. During the selective wet-etching process, the InAs HEMT active layers were protected from the etching solution using the PMMA embedding layer and an $In_{0.53}Ga_{0.47}As$ etch-stop layer. After the selective wet-etch process, the InAs HEMT active layers attached on the surface of PDMS stamp are transferred onto SiO_2/Si substrates by the contact printing process. In the contact printing process, the PDMS stamp attaching the InAs HEMT active layers was gently pressed onto the SiO_2/Si substrate by applying a pressure of ∼100 kPa. During the contact printing process, the InAs HEMT layers on the PDMS stamp were transferred onto SiO_2/Si substrates because of the higher surface energy of SiO_2 compared to that of PDMS, resulting in stronger adhesive forces. Subsequently, it was baked in a convection oven at 100 °C for ∼2 h before the peel-off of the PDMS stamp. Finally, the PMMA coating was removed by acetone washing, resulting in InAs HEMT active layers heterogeneously integrated on SiO_2/Si substrate.

Critical factors affecting the physical properties of the transferred InAs HEMT structure are the crystalline quality of the active layers and the bonding interface between the active layers and the SiO_2/Si surface. Figure 1c shows the cross-sectional high-resolution transmission electron microscope (HRTEM) image of the InAs HEMT structure transferred onto the SiO_2/Si (001) substrate. The InAs HEMT active layers are bonded to the SiO_2/Si surface. Figure 1c evidently supports that the active layers of the InAs HEMT maintain excellent crystalline quality, while the InP substrate and 300 nm thick $In_{0.52}Al_{0.48}As$ buffer layer are completely etched away during the epitaxial transfer process. This high selectivity of the etching process is attributed to two factors. First, the use of an etch-resistive PMMA layer for embedment of the InAs HEMT active layers prevents etching into the side of the active layers (Figure S1, Supporting Information). Second, the 20 nm thick $In_{0.53}Ga_{0.47}As$ layer acts as an etch-stop layer, which preserves the InAs channel from further etching. The role of the $In_{0.53}Ga_{0.47}As$ etch-stop layer is verified using a high-angle annular dark field scanning-TEM (HAADF-STEM) and an energy dispersive spectroscope (EDS) line profile across the bonding interface (Figure S2, Supporting Information).

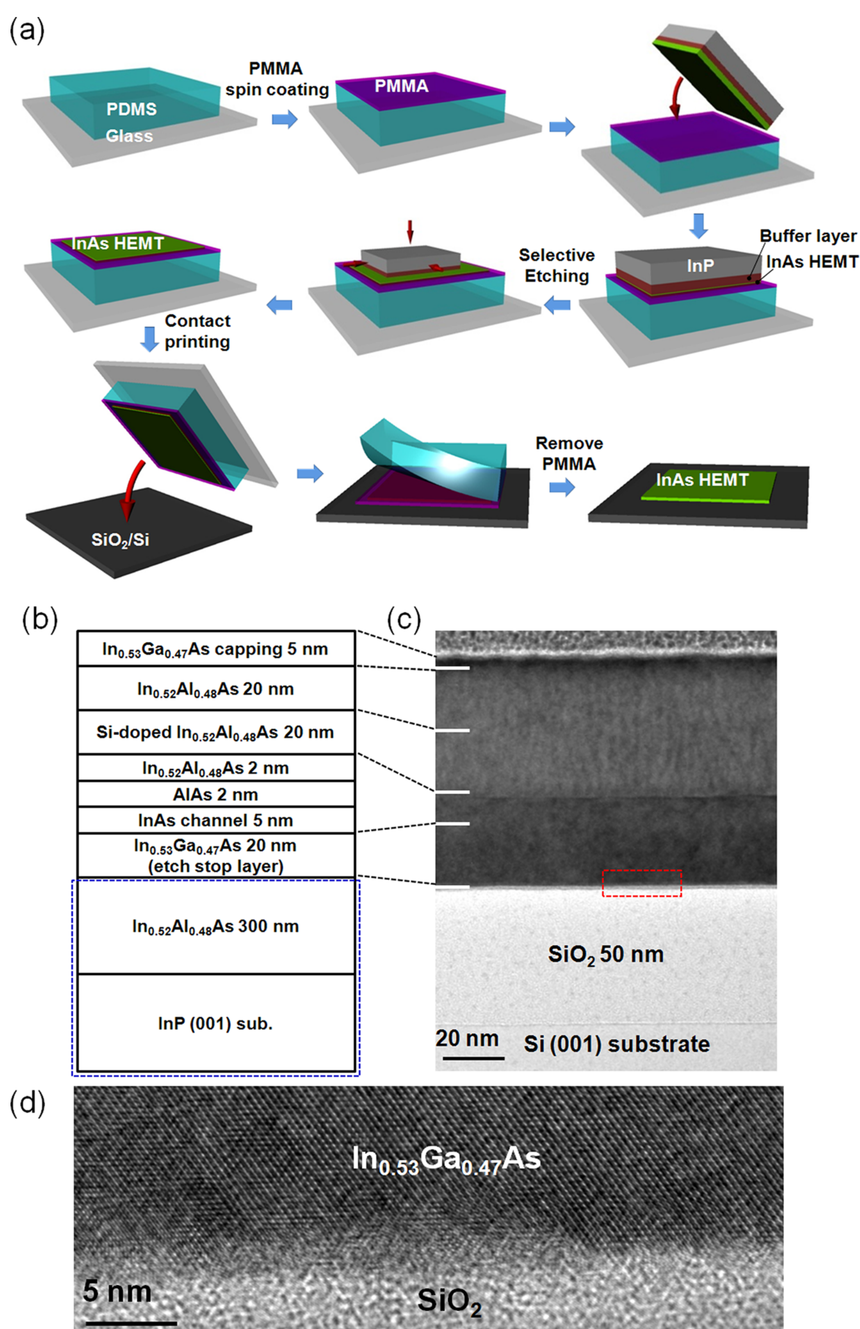

Figure 1. (a) Schematic of the epitaxial transfer processes to heterogeneously integrate an InAs HEMT structure onto a SiO_2/Si substrate *via* selective wet-etching and contact printing. (b) Schematic of an as-grown InAs HEMT structure on an InP (001) substrate. A blue dotted line indicates a portion of the structure etched away. (c) A cross-sectional HRTEM image of an InAs HEMT structure transferred onto a SiO_2/Si substrate. Note that the slight in-plane misorientation between the transferred InAs HEMT structure and the SiO_2/Si substrate obstructs the observation of Si lattices. (d) A magnified HRTEM image focusing on the bonding interface between $In_{0.53}Ga_{0.47}As$ and SiO_2, as indicated in Figure 1c.

The observations illustrate the absolute absence of the $In_{0.52}Al_{0.48}As$ buffer layer at the bonding interface between the $In_{0.53}Ga_{0.47}As$ and SiO_2/Si substrates. Therefore, the $In_{0.53}Ga_{0.47}As$ layer directly bonds to the SiO_2/Si substrate *via* van der Waals interactions. As shown in Figure 1d, the interface between the $In_{0.53}Ga_{0.47}As$ layer and the SiO_2 surface exhibits an extremely flat, sharp edge with no visible defects. The sharp bonding interface is attributed to the high etching selectivity, resulting in an ultrasmooth etch-stopped surface for the $In_{0.53}Ga_{0.47}As$ layer (Figure S3b, Supporting Information). The series of atomic force microscope (AFM) images shown in Figure S3 further support the epitaxial qualities of both InAs HEMT structures, as grown on InP and transferred onto SiO_2/Si with a similar root-mean-square (RMS) roughness of ~0.35 nm. These experimental results prove that multilayered HEMT structures can be successfully

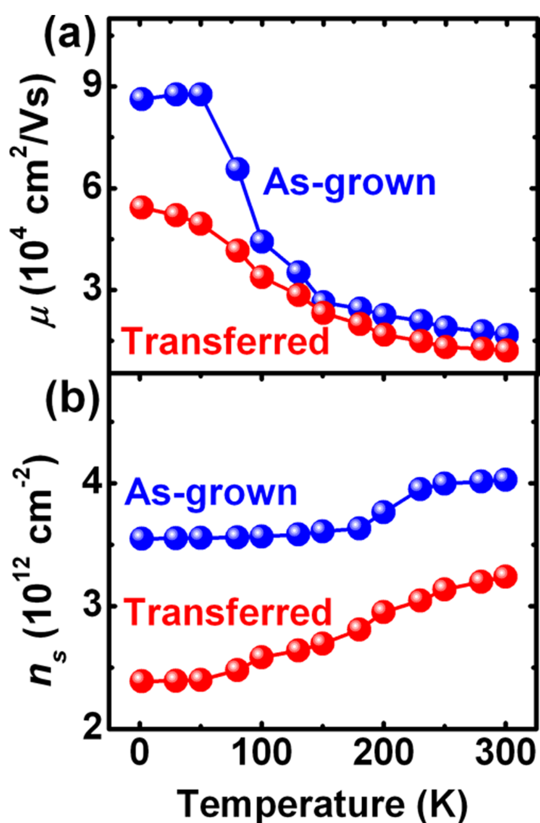

Figure 2. (a) Electron mobility (μ) and (b) sheet carrier concentration (n_s) of as-grown and transferred InAs HEMT structures with respect to temperature ranging from 1.8 to 300 K. Note that the μ values of both InAs HEMT structures are almost the same at room temperature, while the n_s decrease is relatively large; this is favorable for spin-FET applications.

transferred onto Si substrates with minimal defect formation.

We perform Hall measurements to determine electron mobility (μ) and sheet carrier concentration (n_s). Figure 2 shows μ and n_s functions of temperature obtained from the InAs HEMT structures as grown on InP and transferred onto SiO_2/Si substrates. In both cases, the mobility increases as the temperature decreases due to the decreased scatterings from acoustic phonon and interface trap states. The highest μ value of 86200 cm^2/(V s) is obtained from the as-grown InAs HEMT structure with an n_s of 3.56×10^{12} cm^{-2} at 1.8 K. For the transferred InAs HEMT structure, both μ and n_s values are reduced to 54200 cm^2/(V s) with an n_s of 2.39×10^{12} cm^{-2} at 1.8 K. The room-temperature electron mobility of 12100 cm^2/(V s) for the transferred InAs HEMT structure is higher than for $In_{0.53}Ga_{0.47}As$ (6700 cm^2/(V s))[29] and $In_{0.7}Ga_{0.3}As$ (~10000 cm^2/(V s))[19,30] HEMTs grown epitaxially on Si substrates. For all temperature ranges, the transferred InAs HEMT structures display lower μ and n_s values compared to those of as-grown structures, which is attributed to the loss of a 300 nm thick $In_{0.52}Al_{0.48}As$ buffer layer substituted by a 50 nm thick SiO_2 layer with a much larger energy band gap of ~9 eV. A self-consistent Poisson simulation indicates a clear contrast in the energy band diagram between as-grown and transferred structures. The difference between the conduction band minimum and the Fermi level decreases in the transferred structures compared to the as-grown structures. This is attributed to the lower n_s values in the transferred structures compared to those in the as-grown structures. A significant decrease in electron density, from 5.5×10^{18} to 4.8×10^{18} cm^{-3} after the epitaxial transfer, is verified by a band calculation, as discussed later. In fact, the lower n_s value is preferable for spin-FET applications because the probability of spin scattering can be minimized.

The Rashba SOI caused by structural inversion asymmetry (SIA) in the HEMT structures leads to a momentum-dependent effective magnetic field, which facilitates the precession of spin-polarized electrons through a channel.[2] Furthermore, the control of the spin precession by means of an external V_g is an extremely important in spin-FET operation.[3,31] Therefore, the Rashba SOI parameter (α) of the InAs HEMT structures is examined by analyzing the beating patterns observed in the signals of Shubnikov-de Haas (SdH) oscillations. Figure 3a shows the SdH oscillations of the InAs HEMT structure for both cases at 1.8 K without an electric field (V_g = 0 V), where the normalized magnetoresistance (dR_{xx}/dB) for the first derivative of R_{xx} is plotted as a function of the inverse magnetic field (1/B) measured in the presence of perpendicular B. Beating patterns are unambiguously observed from both InAs HEMT structures as-grown on InP and transferred onto SiO_2/Si substrates. The node positions of the beating patterns appear to be due to the existence of two closely spaced frequency components which is attributed to zero-field spin splitting of up and down electron spins. The distance between node positions becomes shorter in the transferred InAs HEMT structure, indicating a stronger Rashba SOI, that is, a larger α. On the other hand, fast Fourier transform (FFT) analysis indicates only two distinct peaks, as shown in Figure 3b, providing further evidence that the beating patterns originate from the spin splitting of electrons. From the node positions of the SdH oscillations in Figure 3a, we calculate the α values to quantitatively compare the Rashba SOI of the two InAs HEMT structures. Using an equation described elsewhere,[31] the α values are estimated to be 8.3 ($\pm$0.5) $\times 10^{-12}$ and 10.9 ($\pm$0.4) $\times 10^{-12}$ eV·m for the as-grown and transferred InAs HEMT structures, respectively. It is surprising that α increases by about 30% in the InAs HEMT transferred onto a SiO_2/Si substrate, despite the loss of the $In_{0.52}Al_{0.48}As$ buffer layer and InP substrate. It is generally known that the α value itself, as well as the V_g dependent α variation, is strongly influenced by the conduction band potential gradient of the channel.[31,32] Therefore, careful study of the band

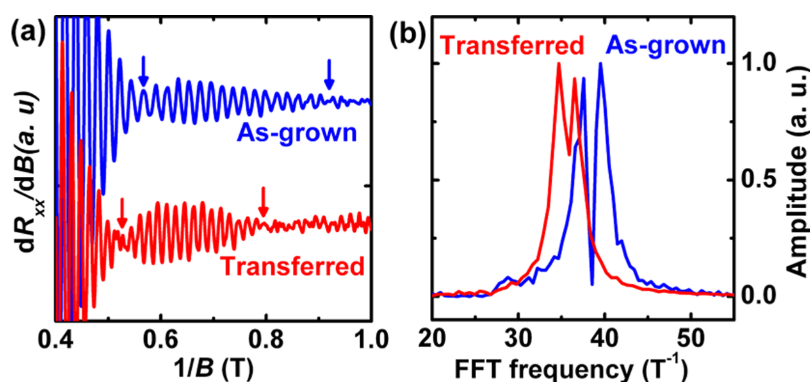

Figure 3. (a) Signals of the SdH oscillation plotted against the inverse magnetic field without a gate electric field (V_g = 0 V) for the as-grown and transferred InAs HEMT structures. Arrows mark the nodes of each beating pattern. (b) Fast Fourier transform of the SdH oscillations in (a). Two frequency peaks indicate that the beating patterns result exclusively from spin splitting.

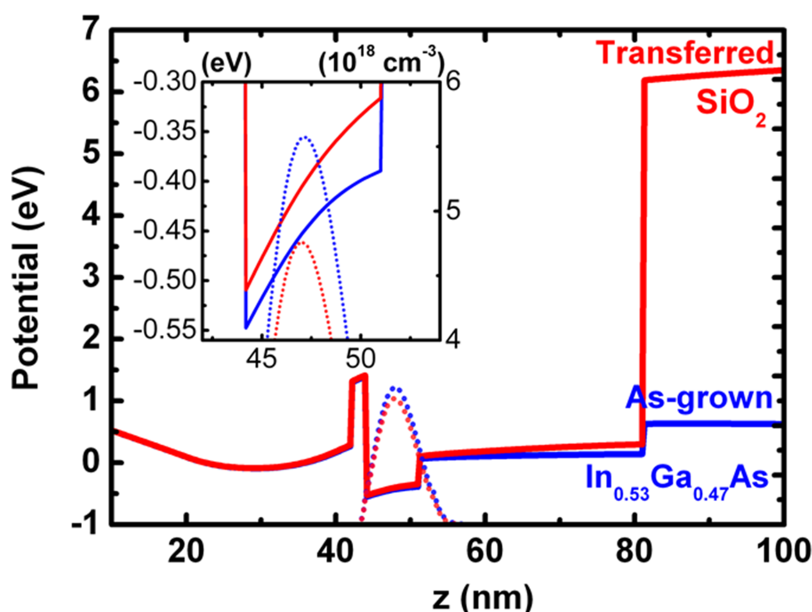

Figure 4. Calculated energy band diagrams (solid lines) and electron distribution (dotted lines) of the as-grown (blue line) and transferred (red line) InAs HEMT structures. The inset is a magnified view of the InAs channel layer to highlight changes in potential height and electron distribution between the two structures.

diagrams is important to thoroughly compare the potential gradient change in the InAs channel for as-grown compared to transferred structures. Figure 4 illustrates the energy band diagrams and electron distribution of the as-grown and transferred InAs HEMT structures. The InAs HEMT active layers bond to SiO_2 and possess a larger band gap of ∼9 eV in the transferred structure, in clear contrast to the 1.45 eV band gap for $In_{0.52}Al_{0.48}As$ in the as-grown structure, leading to a potential height increase from 0.16 to 0.23 eV, as shown in the inset of Figure 4. The potential height increment improves the internal electric field in the InAs HEMT active layers, resulting in an increase in α. This result is very attractive for device applications because a stronger SOI is obtained without an additional doping concentration which usually decreases the spin relaxation length.

The strain relaxation of the InAs channel layer during the epitaxial transfer may be another reason for the improvement in α. The α value is dependent on the band gap of a given channel and the effective mass of the electrons, which can be expressed by the equation below[32]

$$\alpha = b\langle E\rangle \quad (1)$$

where $\langle E\rangle$ is the internal electric field applied to a channel of an HEMT structure and the coefficient b is inversely proportional to the energy gap and the effective mass.[32,33] This equation directly explains the α increase in the InAs HEMT structure transferred onto the SiO_2/Si, as mentioned above. Thus, the band gap and effective mass of the InAs channel should be systematically analyzed to understand the change in α after the epitaxial transfer. Moreover, the strain

relaxation of the InAs channel after the epitaxial transfer should be considered in the analysis. It is generally accepted that the InAs channel layer in the as-grown structure is under compressive strain (InAs a_o = 6.058 Å, $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$/InP a_o = 5.868 Å), while the compressive strain is partially or completely relaxed during the epitaxial transfer process by separation from the extremely thick InP substrate. The band gap and the electron effective mass of the lowest conduction band of InAs with and without strain are obtained from first-principles calculations (see Experimental Section) and compared with experimental results.[34,35] It can be seen clearly in Table 1 that the band gap and effective mass increase with respect to the compressive strain. The elevated band gap and effective mass under compression lead to a reduction in α according to the equation above. After the epitaxial transfer, the compressive strain is reduced compared with before the transfer, resulting in a reduced of the band gap and effective mass as the lattice constant of the InAs channel recovers toward the original cell. Consequently, the increase in α after the transfer can be partly attributed to the relaxation of strain. The decreased effective mass after the transfer can be also attributed to lower n_s in the transferred structure.

TABLE 1. Estimated Energy Band Gap and Effective Mass of the InAs Channel with and without the Compressive Strain[a]

lattice parameter (Å)		band gap (eV)	electron effective mass (m_0)
original cell	6.0588[b]	0.53	0.029
−0.5%	6.0285	0.62	0.034
−1%	5.9982	0.71	0.038
−2%	5.9376	0.89	0.046
−3%	5.8770	1.07	0.055
experimental		0.42[c]	0.023[d]

[a] The first column represents the strain in a percentage with respect to the original cell of a bulk InAs. The experimental values of the band gap and the effective mass for the bulk InAs are shown in the last row. [b] Ref 38. [c] Ref 34. [d] Ref 35.

To date, the α value at V_g = 0 V and the possible reasons for the improvement in α after the epitaxial transfer have been carefully investigated. The most substantial factor for implementation of the spin-FET is gate control of α. In particular, a large variation of α with respect to V_g is important for readier gate modulation across a shorter channel length. Figure 5 exhibits the variation of α manipulated by V_g in the transferred InAs HEMT structure. As mentioned above, two distinct peaks in the FFT are observed exclusively at each V_g, as shown in Figure 5a, indicating that there is no magneto-intersubband scattering over the whole range of the applied gate voltage. Moreover, α monotonically increases with increasing V_g from −3 to +3 V and reaches the highest value of ~13.8 × 10^{-12} eV·m at +3 V, which is one of the highest values ever reported.[36,37] The InAs HEMT structure used in this study is a normal type, in which a carrier supply layer is located above the InAs channel, as opposed to an inverted-type HEMT structure. The normal-type structure with a top gate possesses a positive potential gradient in the InAs channel, as shown in Figure 4, resulting in the increase in α with respect to V_g, as illustrated in Figure 5b. Compared with the inverted-type as-grown InAs HEMT structure,[3] it is obvious that the α values observed in the transferred structure are improved with a similar amount of α variation. The important point is that the normal-type InAs HEMT structure is more favorable for epitaxial transfer because the separation of the InAs HEMT active layers from the original substrate is much easier without loss of the Si-doped $In_{0.52}Al_{0.48}As$ carrier supply layer during the selective wet-etching process. In addition to the significance of gate-controlled α, it is also important for the channel to have a high electron mobility and

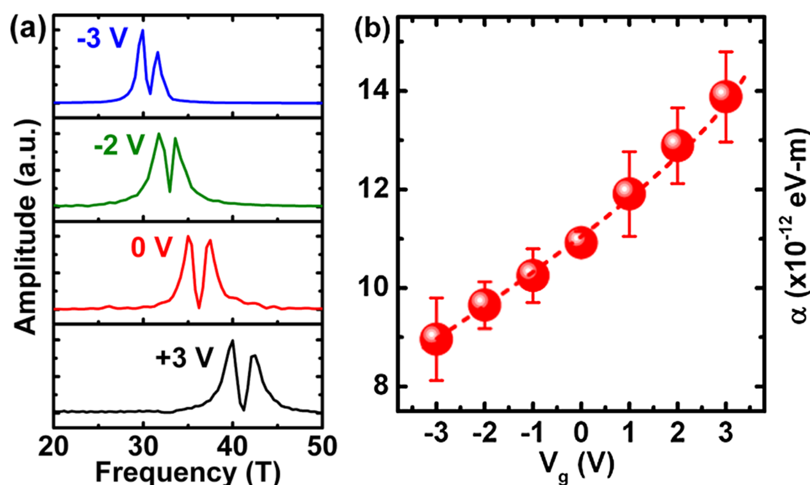

Figure 5. (a) Fast Fourier transform of the InAs HEMT structure transferred onto a SiO_2/Si substrate with respect to the gate electric field (V_g) (b) The Rashba SOI parameter (α) changes as a function of V_g in the InAs HEMT structure transferred onto a SiO_2/Si substrate.

sufficiently long mean free path for high speed and room-temperature operation because the Datta-Das modulation results from a ballistic transport effect.[2,3]

CONCLUSIONS

In conclusion, we have demonstrated gate-controlled Rashba SOI in the InAs HEMT structures epitaxially transferred onto Si substrates for the first time. Using an epitaxial transfer technique, an InAs HEMT structure of high epitaxial quality is exfoliated from a host InP substrate and transferred onto a Si substrate *via* selective wet-etching and contact printing. After the epitaxial transfer, the InAs HEMT maintains excellent interface and crystalline quality with high electron mobility (μ) of 54200 and 12100 $cm^2/(V\ s)$ at 1.8 and 300 K, respectively, which are higher than those of the III−V CS HEMTs epitaxially grown on Si substrates. Furthermore, the SdH oscillation analysis evidently reveals that a Rashba SOI parameter (α) can be manipulated by the gate electric field (V_g). The α in the InAs HEMT transferred onto the Si substrate increased with V_g, reaching $\sim 13.8 \times 10^{-12}$ eV·m at $V_g = +3$ V. The experimental results presented here clearly demonstrate a potential application of spin-FETs that are compatible with Si substrates. Moreover, this work offers a technological platform for the integration of III−V CS heterostructures onto Si substrates by employing an artificial bonding interface, enabling III−V CS heterostructure devices on Si substrates with applications in spintronics, electronics, photovoltaics, and other semiconductor devices.

EXPERIMENTAL SECTION

Epitaxial Growth of InAs HEMT Structures. The fabrication of the InAs HEMT structures was carried out using a molecular beam epitaxy system (MBE, Riber Compact 21T). After being loaded into the system, "epi-ready" semi-insulating InP (001) substrates were heated to 470 °C to thermally desorb a surface oxide layer and subsequently obtain a (2 × 4) surface reconstruction. The streaky (2 × 4) reflection high-energy electron diffraction (RHEED) patterns were kept throughout all layers of the InAs HEMT structure grown at a relatively low growth temperature between 380 and 440 °C. Both $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ layers were completely lattice-matched to an InP (001) substrate. A 20 nm thick $In_{0.53}Ga_{0.47}As$ layer on top of a 300 nm thick $In_{0.52}Al_{0.48}As$ buffer layer was used to exclusively confine electrons in the InAs channel layer and also as an etch-stop layer, which was critical in the selective wet-etching process. A 20 nm thick Si-doped $In_{0.52}Al_{0.48}As$ layer with a doping concentration of $\sim 4 \times 10^{18}$ cm^{-3} functioned as a carrier supply layer and was spatially separated from a 5 nm thick InAs channel layer by a 2 nm thick $In_{0.52}Al_{0.48}As$ layer and 2 nm thick AlAs spacer layers to reduce the ionized donor scattering by the dopant in the carrier supply layer. The 5 nm $In_{0.53}Ga_{0.47}As$ capping layer was used to prevent surface oxidation by the atmosphere.

Epitaxial Transfer Processes. For the transfer of InAs HEMT structures onto Si substrates, we employed an elastomeric PDMS stamp to firmly attach and pick the InAs HEMT layer after the selective wet-etching process and subsequently transfer the InAs HEMT layer efficiently onto Si substrates by providing conformal contacts between the HEMT layer and Si substrates during the contact printing process (Figure 1a).[39]

In the etching process, a PMMA solution (495 PMMA C4, MicroChem, Inc.) is diluted in chlorobenzene (1:2 v/v) to prepare 2 wt % PMMA solution. For the PMMA coating layer, a PMMA solution was spin-coated (4000 rpm, 20 s) on the PDMS. The InP substrate and 300 nm thick $In_{0.52}Al_{0.48}As$ buffer layer were selectively etched in HCl solution (37% HCl diluted in H_2O to a volume ratio of 2.3:1) with the addition of small amounts of a surfactant (sodium dodecyl sulfate, SDS).[40−42] Here, because of the violent reactions in the etching process, the surfactant plays a critical role in preventing bubble formation and attachment on the InP substrates, which otherwise disturbs the uniform etching, resulting in cracks and defects on the InAs HEMT layers after the wet-etching process.[42]

Characterization Methods. The crystalline quality and bonding interface of the InAs HEMT active layers after the epitaxial transfer onto the SiO_2/Si substrates were investigated using a HRTEM operated at 300 kV. The InAs channel was defined into a 64 μm wide and 80 μm long Hall bar pattern (Figure S4, Supporting Information) covered by a 100 nm thick SiO_2 layer for gate insulation. Hall and SdH oscillation measurements were carried out in a 9T-He_4 cryostation to determine the sheet carrier concentration (n_s), electron mobility (μ), and Rashba SOI parameter (α) values.

First-Principles Calculations. The band structure calculation was performed using the Vienna *ab initio* simulation package (VASP) integrated into the MedeA software environment using the Heyd−Scuseria−Ernzerhof (HSE06) hybrid functional.[43−45] The semilocal part was treated within the generalized gradient approximation.[46] Projector augmented-wave pseudopotentials were used.[47] A cutoff energy of 250 eV and a 9 × 9 × 9 k mesh was chosen to ensure the convergence of the band gap and the effective mass. The electron effective mass was evaluated from the parabolic fitting of the lowest conduction band.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Contains details of illustrations of PMMA capping and micrographs during the selective wet-etching process. A Micrograph of a Hall bar pattern, EDS analysis, and AFM analysis. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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